**Code No: A7705** **NR**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**M. Tech I Semester Examinations, APRIL/MAY-2012**
**LOW POWER VLSI DESIGN**
**(EMBEDDED SYSTEMS AND VLSI DESIGN)**

**Time: 3hours** **Max. Marks: 60**

**Answer any five questions**
**All questions carry equal marks**

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1.a) Discuss about recent trends in VLSI circuit design.
b) What are the salient features of SOI technology? Explain.

2.a) With the help of neat sketches, explain about Double diffused Drain and Lightly Doped drain structures.
b) Explain about Punch through in short – channel MOSFETS.

3.a) With the help of neat sketches explain about Deep sub micron processes.
b) What is the need for copper in Integrated circuit fabrication? Explain

4.a) Explain about LEVEL – 1, Slaichman – Hodges SPICE – 3, MOSFET models.
b) What are the features of HSPICE level 50 (Phillip MOS69) Model? Explain.

5.a) Explain about the Temperature – Dependant Hybrid – Mode Device Threshold Voltage Model.
b) With a Schematic diagram explain about space – charge current is MOSFETS.

6.a) Draw the circuit for Full – Swing complementary MOS/ Bipolar two input NAND gate and explain about the same.
b) Draw the circuit for FS – CMBL two – input MAND gate with positive feed back.

7.a) Draw the circuit for a $B_1$ CMOS charge pump integrated High $\beta$ – $B_I$CMOS and explain its operation.
b) Give the performance analysis of High $\beta$ $B_1$CMOS circuits.

8. Write notes on any TWO
a) Low Power Flip – Flops
b) Quality measures for Low power Latches
c) BSIMS 3, Version 3 Current Model

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